PATENT No. 7,045,413 Attorney's Doc. No. 8750-057

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE.

In re Patent No.: 7.045.413

Inventor: Sang-Eun LEE, et al.

Issued: May 16, 2006

 Ser. No.:
 10/773,805
 Filed:
 February 5, 2004

 Group Art Unit:
 2811
 Examiner:
 Steven LOKE

For: METHOD OF MANUFACTURING A SEMICONDUCTOR

INTEGRATED CIRCUIT USING A SELECTIVE DISPOSABLE SPACER TECHNIQUE AND SEMICONDUCTOR INTEGRATED

CIRCUIT MANUFACTURED THEREBY

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents P.O. Box 1450

Alexandria, VA 22313-1450

Upon comparison of the above-identified original Letters Patent with applicant's copy of the application, the following errors, <u>made by the USPTO</u>, in the original Letters Patent has been noted:

Column 8, line 15, the word "3b" should read -- 37b --.

Applicant respectfully requests that a Certificate of Correction calling attention to the above error be issued pursuant to Rule 322 of the Patent Office and Title 35, United States Code, Section 254.

Respectfully submitted,

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UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

Page	1	of	1

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APPLICATION NO.: 10/773,805

ISSUE DATE : May 16, 2006

INVENTOR(S) : Sang-Eun LEE, et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 8, line 15, the word "3b" should read - 37b --.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

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